REMARKS

This is a reply to the outstanding Office Action (first action on the merits) dated April 1, 2002, in which concurrently filed herewith is a Petition for Extension of Time covering the two month extended time period for filing this response including the required fee amount thereof. (A completed credit card authorization form is enclosed herewith, covering the fee amount for the extension of time.)

By the amendments presented hereinabove, claims 1-5, 12, 15-17 and 39-42 were amended and claims 51-54 were newly presented. (While applicants have presently canceled the previously non-elected claims for purposes of avoiding an added claim fee with the present submission, they are reserving their right to subsequently file a divisional application directed thereto.)

The amendments made to the original claims are in consideration of further highlighting the particularities of the method directed to the manufacture of a semiconductor integrated circuit device such as that covered by the pending claimed subject matter including in terms of more clearly defining the same over the art documents, as cited in the outstanding art rejection. For example, language was added to a number of the independent claims directed to the polishing and cleaning of the insulating film surface such as prior to the formation of a CAP conductive film associated with a wiring to remove foreign matter or contaminated metal including any remaining conductive film outside of the groove for wiring from the insulating film. Variations of this featured aspect are now contained in connection with the method of manufacture called for in each of independent claims 1-5 and 39. Revisions were also made in connection with further defining the process steps such as with regard to the part thereof associated with the removal of the barrier layer and conductive film from outside of the groove for wiring by polishing. This can be seen

in connection with Fig. 7(a) such as it relates to example embodiment 1 of the present application, although not limited thereto, in which both the titanium nitride (TiN) barrier layer 26a and copper film 26b are removed from surfaces outside of the grooves for wiring such as by the CMP method to thereby form wiring 26, which is contained in grooves associated with that wiring layer.

With regard to independent claim 1 as well as other ones of the independent claims presently being amended, the manufacturing step associated with the formation of a barrier layer and a conductive film over the insulating film including inside of the groove for wiring and followed by the removal of the same from outside of the groove for wiring by polishing is now also called for with regard to other ones of the independent claims. Additionally, the step directed to the forming of a cap conductive film such as tungsten film 26c, such as it relates to the method associated with the manufacture of the example embodiment 1, although not limited thereto, is now further defined as a cap conductive film (e.g., 26c) formed on the wiring (e.g., 26) in self-alignment with the wiring by selective growth or preferential growth of the cap conductive film on that wiring. Since tungsten is formed on the wiring (e.g., 26) by selective growth or preferential growth, the wiring 26 is not directly in contact on the upper surface of the wiring with the insulating films, such as the silicon nitride film and the silicon oxide film. Rather, the wiring is in contact with the cap conductive film (e.g., tungsten film 26c) which leads to significant electromigration reduction as well as a number of other significant improvements. (See the related discussion on page 18, paragraph [0081] to page 20, paragraph [0089], Figs. 22(a)-24(b), 27 and 28, and so forth). The following discussion is directed to a number of the key featured aspects of the present claimed subject matter.

As can be seen from Figs. 27(a) and 28(a), when contaminant metal remains on the insulating film (e.g., 23, 33 of example embodiment 1) after polishing by CMP of the copper film (e.g., 26b, 35b) and the like, the cap conductive film (e.g., 26c, 35c) would undesirably grow on the contaminant metal remaining on the insulating film (e.g., 23, 33) during the selective deposition step of tungsten. This would result from a breakdown of selectivity which may lead to a lower yield due to, for example, short-circuiting. The present invention, however, overcomes this. That is, after completion of the polishing of the copper by CMP such as it relates to step (b) of claim 1, etc., the substrate surfaces (including the surfaces of the copper film 26b, 35b and the silicon oxide film 23, 33) are cleaned with a cleaning solution such as a solution for removing foreign matter and contaminant metals, after which the cap conductive films (e.g., tungsten films 26c, 35c, although other conductive film layers may be used) are formed on the wirings 26, 35 by selective or preferential growth. Through employing such cleaning process of the, for example, "first insulating film" (e.g., 23, 33) prior to forming a "cap conductive film", according to step (d), of claim 1, etc., good selectivity/preferential ability is ensured in connection with the formation of the cap conductive films (26c, 35c) (see Fig. 27(c) and on page 40, paragraphs [0168] – [0170] of the Substitute Specification.) Although the cap conductive film associated with each of the wiring layers is featured as a tungsten (W) film in the example embodiments, other types of conductive film layers may be used in the formation of the cap conductor including, but not limited to, TiN, Ta, TaN, WN or Ni film, such as discussed on page 18, paragraph [0084] of the Substitute Specification.

Consistent with the present invention, according to independent claims 1-5 and 39, using embodiments 5 and 6 as examples thereof, although not limited

thereto, after forming the copper film (e.g., 26b, 36b) and after polishing by the CMP method, foreign matter and contaminant metal such as copper that remained are removed by cleaning the surface of the insulating film (e.g., 23, 33) by a cleaning process such as that called for according to step (c) in claims 1 and 2, step (j) according to the method in claim 3, step (g) according to the method in claims 4 and 5 and step (d) according to the method in claim 39, so that the yield including the short-circuiting yield is improved (see Figs. 27-28, and on page 40, paragraphs [0165] - [0171] related to the fifth embodiment and paragraphs [0175] – [0176] related to the example sixth embodiment of the present application). As to the cleaning process employed, an example of details thereof is given in connection with claims 15-16, 41, 51 and 52. In the example fifth embodiment, it is noted that such cleaning process is performed by using a solution which includes at least one of hydrogen fluoride (HF), citric acid, hydrogen peroxide (H_2O_2), etc. With regard to the sixth embodiment, such cleaning is effected by the reduction treatment (hydrogen annealing, ammonia plasma). (Example embodiment six is discussed from page 41, paragraph [0172] – page 44, [0181].) By performing both the cleaning process using a solution such as in connection with the example fifth embodiment as well as the reduction treatment such as in connection with the example sixth embodiment, the reliability of the copper wiring is improved significantly (page 44, paragraph [0181], of the Substitute Specification).

According to a further aspect of the invention, additional cleaning is performed subsequent to the formation of the cap conductive film. For example, as shown with regard to the example seventh embodiment, and discussed in paragraphs [0182] – [0190], covering pages 44 – 45 of the Substitute Specification, after the selective or preferential growth of the tungsten film (e.g., 26c, 35c) on the wiring (e.g., 26, 35), a

cleaning step is added in the process, namely, the surface of the insulating film (e.g., 23, 33) is cleaned such as with a cleaning solution so as to enhance the reliability of the Cu wiring. This featured aspect is contained in dependent claims 17, 40, step (f) in claim 43 and in claims 53 and 54, for example. It is submitted, the invention as now called for in independent claims 1-5, 39, 43, 47 and 49 and further according to the corresponding dependent claims thereof could not have been rendered obvious even in view of the combined teachings of Omura and Uozumi. Therefore, insofar as presently applicable, the standing rejection under 35 USC §103(a) is accordingly traversed and reconsideration and withdrawal of the same is respectfully requested.

Omura disclosed a method which includes fabricating also a cap layer (e.g., 60d, 60s) on interconnect grooves (e.g., 44S, 44D) (See Figs. 15-16). In accordance with Omura's scheme, cap layer 60 covers the interconnect grooves 44S, 44D, while leaving exposed the insulating film 44. (Column 13, lines 66, to column 14, line 1, in Omura.) After the cap layer 60 is formed, rapid thermal annealing takes place in an N_2 atmosphere to improve heat resistance and barrier performance of the cap layer. (Column 14, lines 21-26, of Omura.) Next, the cap layer becomes partially removed by CMP so as to planarize the surface thereof, while leaving the first and second portions (e.g., 60s, 60d) of the cap layer 60 in the interconnect grooves 44S, 44D, respectively. (Column 14, lines 46-50, in Omura.) Stated differently, the cap layer such as the first and second portions thereof 60s, 60d, are not selectively grown only in the interconnect layer, as is called for in the presently pending independent claims 1-5, 39, 42. It is submitted, Omura, clearly, failed to teach such key featured aspects which are called for, among other featured aspects thereof, in the independent claims.

Uozumi, it is submitted, is similarly deficient as to the present claimed subject matter. Uozumi's disclosure features a method of fabricating a barrier metal on the surface of a copper Cu layer (e.g., barrier metal layer 4 and Cu layer 3). A barrier metal layer is included in Uozumi's scheme such as metal layer 2, which is formed on the side wall of each wiring groove which surrounds a buried copper layer 3. A copper oxide film 5 is formed on the surface of copper film 3 in Uozumi, by adjusting the solution mixture of aqueous ammonia and aqueous hydrogen peroxide in such a way as to achieve a PH of 10 or less. The copper oxide film 5 is etched without roughening the copper surface by adjusting the solution mixture of aqueous ammonia and aqueous hydrogen peroxide so as to achieve a PH factor of greater than 10. Therefore, there is formed a wiring groove on the upper portion of the copper layer 3.

Uozumi also disclosed a barrier metal layer 4 deposited on the upper portion of the copper layer 3 by sputtering, CVD or the like. Further, polishing of the barrier metal layer 4 out of the wiring groove by a CMP process is effected to bury the barrier metal 4 in a wiring groove on the upper portion of the copper layer 3. That is, Uozumi's scheme does not teach, it is submitted, that his layer 4 is that of a barrier metal layer as that presently called for. Uozumi disclosed a scheme in which a copper oxide film 5 and a wiring groove is formed by etching the copper oxide film 5. Also, polishing by CMP process is effected after depositing the barrier metal 4, according to Uozumi, thereby increasing the number of manufacturing steps. Such manufacturing steps as that just discussed, regarding Uozumi's process, are considered unnecessary to achieve our invention which calls for selectively growing the barrier metal 4 on the copper wiring. It is clearly apparent, therefore, in view of at least the above-noted deficiencies in both Uozumi and Omura, one of ordinary skill,

clearly, could not have been led to achieve the present invention. Therefore, the present invention could not have been rendered obvious from the combined teachings of Ouzumi and Omura.

Therefore, in view of the amendments presented hereinabove, together with these accompanying remarks, reconsideration as well as favorable action therefor on all the presently pending claims and an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (501.39868X00).

Respectfully submitted,
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Version With Markings To Show Changes Made

Please **amend** claims 1-5, 12, 15, 16, 17 and 39-42 as follows:

1. (Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a groove for wiring in a first insulating film formed on a semiconductor substrate;

(b) successively forming a barrier layer and a conductive film over said first insulating film including the inside of said groove for wiring and removing said barrier layer and said conductive film from outside of said groove for wiring by polishing, thereby forming a wiring;

(c) cleaning a surface of said insulating film to remove conductive film that remains on said first insulating film in said step (b);

[(c)] (d) forming a cap conductive film on said wiring by selective growth or preferential growth of said cap conductive film on said wiring; and

[(d)] (e) forming a second insulating film over said cap conductive film and said first insulating film.

2. (Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a groove for wiring in a first insulating film formed on a semiconductor substrate;

(b) successively forming a barrier layer and a [first] conductive film over

said first insulating film including the inside of said groove for wiring [to form] and removing said barrier layer and said conductive film from outside of said groove for wiring by polishing, thereby forming a wiring;

(c) cleaning a surface of said insulating film to remove conductive film that remains on said first insulating film in said step (b);

[(c)] (d) forming a cap conductive film on said wiring in self-alignment with said wiring by selective growth or preferential growth of said cap conductive film on said wiring;

[(d)] (e) forming a second insulating film over said cap conductive film and said first insulating film;

[(e)] (f) partly removing said second insulating film on said wiring to form an opening so that said cap conductive film is exposed; and

[(f)] (g) forming a second conductive film in said opening.

3. (Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first wiring on a semiconductor substrate;

(b) forming a first insulating film on said first wiring;

(c) removing said first insulating film at a portion thereof corresponding to a contact region of said first wiring to form a contact hole;

(d) forming a first conductive film over said insulating film including the inside of said contact hole;

(e) removing said first conductive film from outside of said contact hole to form a plug;

(f) forming a second insulating film over said first insulating film and said

plug;

(g) removing said second insulating film at a portion thereof corresponding to a region where a second wiring is to be formed, thereby forming a groove for wiring;

(h) successively forming a barrier layer and a second conductive film on said second insulating film including the inside of the said groove for wiring;

(i) removing said barrier layer and said second conductive film from outside of said groove for wiring by polishing to form a second wiring;

(j) cleaning a surface of said second insulating film to remove said second conductive film that remains on said second insulating film in said step (i);

[(j)] (k) forming a cap conductive film on said second wiring in self-alignment with said second wiring by selective growth or preferential growth of said cap conductive film on said second wiring; and

[(k)] (l) forming a third insulating film over said cap conductive film and said second insulating film.

4. A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first wiring on a semiconductor substrate;

(b) successively forming a first insulating film and a second insulating film on said first wiring;

(c) removing said first insulating film and said second insulating film at a portion thereof corresponding to a contact region of said first wiring to form a contact hole;

(d) removing said second insulating film at a portion thereof

corresponding to a region where a second wiring is to be formed thereby forming a groove for wiring;

(e) successively forming a barrier layer and a conductive film on said second insulating film including said contact hole and the inside of the said groove for wiring;

(f) removing said barrier layer and said conductive film from outside of said contact hole and said groove for wiring by polishing to form a second wiring and a connection between said first wiring and said second wiring;

(g) cleaning a surface of said second insulating film to remove said second conductive film that remains on said second insulating film in said step (f);

[(g)] (h) forming a cap conductive film on said second wiring in self-alignment with said second wiring by selective growth or preferential growth of said cap conductive film on said second wiring; and

[(h)] (i) forming a third insulating film over said cap conductive film and said second insulating film.

5. A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first wiring on a semiconductor substrate;

(b) successively forming a first insulating film and a second insulating film on said first wiring;

(c) removing said second insulating film at a portion thereof corresponding to a region where a second wiring is to be formed to form a groove for wiring;

(d) removing said first insulating film at a portion thereof corresponding to

a contact region of said first wiring thereby forming a contact hole;

(e) successively forming a barrier layer and a conductive film on said second insulating film including said contact hole and the inside of the said groove for wiring;

(f) removing said barrier layer and said conductive film from outside of said contact hole and said groove for wiring <u>by polishing</u> to form a second wiring and a connection between said first wiring and said second wiring;

<u>(g) cleaning a surface of said second insulating film to remove said second conductive film that remains on said second insulating film in said step (f);</u>

[(g)] <u>(h)</u> forming a cap conductive film on said second wiring <u>in said self-alignment with said second wiring</u> by selective growth or preferential growth of said cap conductive film on said second wiring; and

[(h)] <u>(i)</u> forming a third insulating film over said cap conductive film and said second insulating film.

12. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 1, wherein said second insulating film is formed by the steps of:

(a) forming, on said cap conductive film, a diffusion-preventing insulating film for preventing the diffusion of a conductor material constituting said cap conductive film; and

(b) forming, <u>on</u> said diffusion-preventing insulating film, a low dielectric insulating film whose dielectric constant is lower than said diffusion-preventing insulating film.

15. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 1, wherein said [cap conductive film is formed after cleaning substrate surfaces with] cleaning in said step (c) is performed by using a solution containing at least one of hydrogen fluoride (HF) [or a solution capable of removing foreign matters or a contaminant metal] , citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid (H_4SO_4), and ammonia (NH_3).

16. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 1, wherein said [cap conductive film is formed after treatment of] step (c) includes a sub-step of treating substrate surfaces with hydrogen.

17. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 1, wherein [the step of forming said cap conductive film] said step (d) includes [the step] a sub-step of cleaning substrate surfaces with a solution containing at least one of hydrogen fluoride (HF), hydrogen peroxide (H_20_2) and citric acid[, or a solution capable of removing foreign matters or a contaminant metal] after the selective growth or preferential growth of said cap conductive film.

39. (Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a groove in a first insulating film formed on a semiconductor substrate;

(b) depositing [a] a first conductive film comprising copper [film] as a main component thereof on said first insulating film including the groove;

(c) removing said [copper] first conductive film from outside of said groove by polishing to bury said first conductive [copper] film in said groove; [and]

(d) cleaning with a solution capable of removing a foreign matter or a contaminant metal from a surface of said first insulating film to remove said contaminant metal that remains on a surface of said first insulating film in said step (c); and

[(d)] (e) forming a cap conductive film on said [copper] first conductive film in said groove in self-alignment with said first conductive film by selective growth of the cap conductive film on said [copper] first conductive film buried in said groove by a selective CVD (chemical vapor deposition) method.

40. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 39, further comprising, after [the] said step [of (d)] (e), cleaning with a solution capable of removing a foreign matter or a contaminant metal.

41. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim [40] 39, [further comprising, between the steps of (c) and (d), cleaning with a solution capable of removing a foreign matter or a contaminant metal] wherein said cleaning in said step (d) is a cleaning with a solution containing at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid and ammonia (NH_3).

42. (Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 39, wherein said cap conductive film is made of a

tungsten film.